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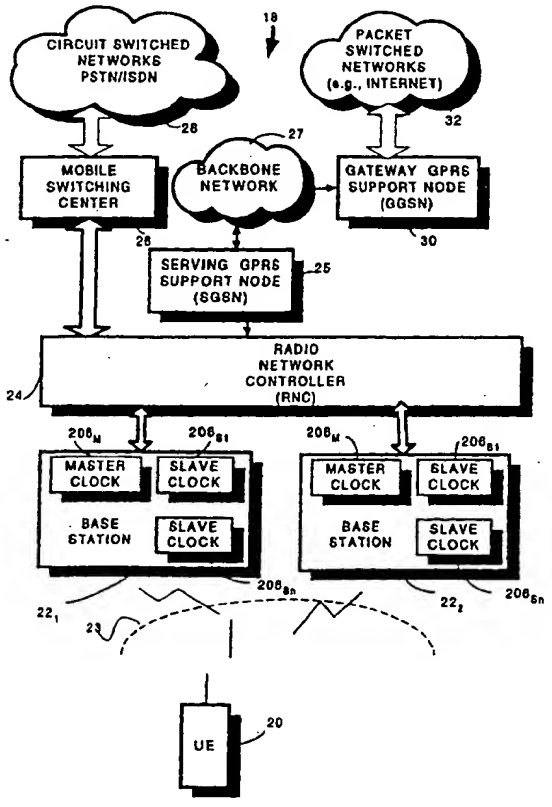
(54) Title: CLOCK SYNCHRONIZATION IN TELECOMMUNICATIONS NETWORK USING SYSTEM FRAME NUMBER

(57) Abstract

A telecommunications system (18) capitalizes employment of a system frame number (SFN) for synchronizing plural real time clocks (206) provided at one or more nodes of the network. System frame signals (e.g., pulses) are distributed from a source (210, 310) to processors (202) having slave clocks (206_S) that need to be synchronized with a master clock. A master processor (202_M, 302_T) sends a clock set message (500) to the processors, the clock set message including a reference master clock time (506) and a reference system frame number (504). The recipient processors which receive the clock set message resynchronize their respective slave clocks using the reference master clock time and the reference system frame number. In one mode, the clock set message directs the recipient processors to set their respective slave clocks to the reference master clock time upon the recipient processors obtaining the reference system frame number. In another mode, the clock set message advises the recipient processors of an actual master clock time at the reference system frame number, thereby enabling the recipient processor to calculate an adjusted slave clock time.



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CLOCK SYNCHRONIZATION IN TELECOMMUNICATIONS NETWORK USING SYSTEM FRAME NUMBER

1. FIELD OF THE INVENTION

The present invention pertains to telecommunications, and particularly to the synchronization of real time clocks maintained by plural processors of a telecommunications network.

2. RELATED ART AND OTHER CONSIDERATIONS

Cellular telecommunications systems employ a wireless link (e.g., air interface) between a (mobile) user equipment unit and a base station (BS) node. The base station node has transmitters and receivers for radio connections with numerous user equipment units. One or more base station nodes are connected (e.g., by landlines or microwave) and managed by a radio network controller node (also known in some networks as a base station controller [BSC]). The radio network controller node is, in turn, connected through control nodes to a core communications network. Control nodes can take various forms, depending on the types of services or networks to which the control nodes are connected. For connection to connection-oriented, switched circuit networks such as PSTN and/or ISDN, the control node can be a mobile switching center (MSC). For connecting to packet switching data services such as the

Internet (for example), the control node can be a gateway data support node through which connection is made to the wired data networks, and perhaps one or more serving nodes.

A telecommunications connection between a mobile user equipment unit and another party (e.g., in the core communications network or another mobile user equipment unit) thus involves an uplink from the mobile unit through a base station and a radio network controller (RNC), and a downlink in the reverse direction. In some types of telecommunications systems, control and user information is transmitted in frames both on the uplink and downlink.

In handling the transmission of frames and other activities, some of the nodes of cellular telecommunications networks employ plural processors, each having a real time operating system with a real time clock. It is important, in maintaining control of the telecommunications network and in handling connections, that the real time clocks be synchronized. What is needed, therefore, and an object of the present invention, is a technique for synchronizing real time clocks in a telecommunications network.

BRIEF SUMMARY OF THE INVENTION

A telecommunications system capitalizes employment of a system frame number for synchronizing plural real time clocks provided at one or more nodes of the network. System frame signals (e.g., pulses) are distributed from a source (e.g., oscillator) to devices or units having slave clocks that need to be synchronization with a master clock. A master processor sends a clock set message to the processors, the clock set message including a reference master clock time and a reference system frame number. The recipient processors which receive the clock set message resynchronize their respective slave clocks using the reference master clock time and the reference system frame number. In one mode, the clock set message directs the recipient processors to set their respective slave clocks to the reference master clock time upon the recipient processors obtaining the reference system frame number. In another mode, the clock set message advises the recipient processors of an actual master clock time at the reference system frame number, thereby enabling the recipient processor to calculate an adjusted slave clock time.

The location of the master processor relative to the recipient processors varies in accordance with differing embodiments. For example, in one embodiment, the master processor and the recipient processors are located at a same node of the telecommunications network, e.g., a base station node. In such embodiment, the master processor and the recipient processor can be located on differing device boards at a same node of the telecommunications network. In another embodiment, the master processor and the recipient processor are located at differing nodes of the telecommunications network, e.g., the master processor is located at a radio network controller node and one or more recipient processors are located at a base station node of the telecommunications network.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other objects, features, and advantages of the invention will be apparent from the following more particular description of preferred embodiments as illustrated in the accompanying drawings in which reference characters refer to the same parts throughout the various views. The drawings are not necessarily to scale, emphasis instead being placed upon illustrating the principles of the invention.

Fig. 1 is a schematic view of an embodiment of a telecommunications system which utilizes the present invention.

Fig. 2 is a schematic view showing employment of a synchronization technique of the present invention at a base station.

Fig. 3 is a schematic view showing employment of a synchronization technique of the present invention between a radio network controller (RNC) and a base station.

Fig. 4A is a flowchart showing a first mode of using a clock set message (CSM) of the present invention.

Fig. 4B is a flowchart showing a second mode of using a clock set message (CSM) of the present invention.

Fig. 5 is a diagrammatic view of an example format of a clock set message (CSM) of the present invention.

DETAILED DESCRIPTION OF THE DRAWINGS

In the following description, for purposes of explanation and not limitation, specific details are set forth such as particular architectures, interfaces, techniques, etc. in order to provide a thorough understanding of the present invention. However, it will be apparent to those skilled in the art that the present invention may be practiced in other embodiments that depart from these specific details. In other instances, detailed descriptions of well known devices, circuits, and methods are omitted so as not to obscure the description of the present invention with unnecessary detail.

Fig. 1 shows a telecommunications network 18 in which a user equipment unit 20 communicates with one or more base stations 22 over air interface (e.g., radio interface) 23. Base stations 22 are connected by terrestrial lines (or microwave) to radio network controller (RNC) 24 [also known as a base station controller (BSC) in some networks]. The radio network controller (RNC) 24 is, in turn, connected through a control node known as the mobile switching center 26 to circuit-switched telephone networks (PSTN/ISDN) represented by cloud 28. In addition, radio network controller (RNC) 24 is connected to Serving GPRS Support Node (SGSN) 25 and through backbone network 27 to a Gateway GRPS support node (GGSN) 30, through which connection is made with packet-switched networks (e.g., the Internet, X.25 external networks) represented by cloud 32.

As understood by those skilled in the art, when user equipment unit 20 participates in a mobile telephonic connection, signaling information and user information from user equipment unit 20 are transmitted over air interface 23 on designated radio channels to one or more of the base stations 22. The base stations have radio transceivers which transmit and receive radio signals involved in the connection or session. For information on the uplink from the user equipment unit 20 toward the other party involved in the connection, the base stations convert the radio-acquired information to digital signals which are forwarded to radio network controller (RNC) 24. The radio network controller (RNC) 24 orchestrates participation of the plural base stations 22 which may be involved in the connection or session, since user equipment

unit 20 may be geographically moving and handover may be occurring relative to the base stations 22. On the uplink, radio network controller (RNC) 24 picks frames of user information from one or more base stations 22 to yield a connection between user equipment unit 20 and the other party, whether that party be in PSTN/IDSN 28 or on the packet-switched networks (e.g., the Internet) 32.

The example embodiments illustrated herein happen to employ code division multiple access (CDMA), wherein the information transmitted between a base station and a particular mobile station is modulated by a mathematical code (such as spreading code) to distinguish it from information for other mobile stations which are utilizing the same radio frequency. Thus, in CDMA, the individual radio links are discriminated on the basis of codes. Various aspects of CDMA are set forth in Garg, Vijay K. et al., *Applications of CDMA in Wireless/Personal Communications*, Prentice Hall (1997). In view of the diversity aspects of CDMA, the user equipment unit 20 in Fig. 1 is depicted as being in contact with multiple base stations 22 (e.g., base station 22_1 and base station 22_2).

The present invention particularly pertains to synchronization of real time clocks in a telecommunications network 18 wherein the information is transmitted in frames or information packets both on the uplink and on the downlink. Each frame is consecutively numbered to include an identifying frame number (FN). The frame number (FN) is, in turn, based on a system frame number (SFN) which is maintained at both the base stations 22 and the radio network controller (RNC) 24.

The SFN is synchronized between the radio network controller (RNC) 24 and the base stations 22. In this regard, each base station 22 has a system frame number (SFN) oscillator which distributes the system frame number to all boards in the base station 22. Thus, when a base station 22 starts up, this SFN oscillator is synchronized with the radio network controller (RNC) 24, and thereafter each base stations 22 keeps it own SFN counter using the SFN oscillator. Thereafter, when the radio network controller (RNC) 24 sends a user data frame to the base station 22 for eventual forwarding to the user equipment unit 20, every frame is marked with the frame number (FN). This frame number (FN) is actually derived from the SFN, e.g., SFN mod 72. Using this frame number FN, and the SFN kept by the base station 22, the base station 22 can send the frame at the specified time.

The real time clock synchronization of the present invention applies to numerous embodiments, of which Fig. 2 provides a first example. In particular, Fig. 2 illustrates a representative base station 22 of telecommunications network 18. The example base station 22 of Fig. 2 comprises plural units or device boards 200_M, 200_{S1}, ...200_{Sn}. Each device board 200 has a board processor 202, which executes a real time operating system (RTOS) 204 having a real time clock 206.

In Fig. 2, device board 200_M is denominated as a "master board" by virtue of the fact that its real time clock 206_M is considered the master real time clock (master clock 206_M). In addition, in the illustrated embodiment, device board 200_M includes a source of system frame signals, i.e., SFN oscillator 210. The processor 202_M of master board 200_M communicates via interface 212 and over a control bus 214 with processors of other device boards 200.

In the example of Fig. 2, the device boards 200 other than master device board 200_M are herein known as slave boards solely for their respective roles in the synchronization of the invention. Respecting synchronization, the real time clocks 206 on slave boards 200_{S1} - 200_{Sn} are slaved to the master clock 206_M. In addition, slave boards 200_{S1} - 200_{Sn} receive the system frame signals from SFN oscillator 210 over SFN signal line 216.

In the illustrated embodiment, the SFN oscillator 210 outputs a pulse which in the illustrated embodiment occurs every 10 milliseconds. The pulses issued from SFN oscillator 210 are applied to a SFN counter 220 in each of the slave boards 200_{S1} - 200_{Sn}. The SFN counter 220 maintains a count of the pulses comprising the system frame signals received on SFN signal line 216. In addition, the master processor 202_M receives and counts the system frame signals. When the master processor 200_M determines that a complete set of system frame signals has been issued by SFN oscillator 210, the master processor 200_M issues a reset signal on reset line 222.

The slave boards 200_{S1} - 200_{Sn} each have one or more characteristic functions, represented generally by function blocks 230_{S1} - 230_{Sn} resident on the respective boards. Each of the function blocks 230_{S1} - 230_{Sn} can perform one or more base station functions. For example, function block 230_{S1} can be a transmitter/receiver for effecting communication over air interface 23. The function block 230_{Sn} can be an interface to

another node of telecommunications network 18 (such as radio network controller (RNC) 24 , for example), in which case device board 200_{Sn} functions as an extension board. Likely several of the device boards 200 of base station 22 serve as transmitter/receiver boards. However, the particular identities and mix of functions provided at base station 22 are not germane to the present invention, with the aforementioned functions being provided for sake of illustration.

It should be understood that Fig. 2 does not illustrate the transmission of user data frames and the like between the device boards 200 of base station 22. Such transmission of user data frames can occur in any conventional manner, such as by encapsulation in ATM frames, for example. Accordingly, in some embodiments a switch, such as an ATM switch, can be provided for facilitating transmission of, e.g., user data frames between device boards of base station 22.

The present invention seeks to synchronize the slave clocks 206_S to the master clock 206_M. It is presumed that the master clock 206_M has been accurately maintained or kept (e.g., by radio network controller (RNC) 24), and that the SFN counter of the master processor has been appropriately synchronized (e.g., upon start up). The synchronization of the present invention capitalizes upon the system frame numbers (SFNs) that are maintained at the various device boards 200 of telecommunications network 18. In this regard, and as mentioned above, the SFN oscillator 210 outputs pulses on line 216. The pulses on line 216 are counted by the SFN counters 220 so that each device board 200, so that knowing the frame number (FN) of each user data frame and the SFN the device board 200 can send the frame over the air interface at the proper time. In addition, the master processor 202_M counts the system frame pulses and determines when the system frame number should be reset to zero. When the master processor 202_M determines that the system frame number should be reset to zero, it sends a reset signal on line 222.

In accordance with the present invention, the master processor 202_M sends a clock set message (CSM) 500 on control bus 214 to recipient processors 202_S on each of the slave boards 200_{S1} - 200_{Sn}. An example format of a representative clock set message (CSM) 500 is illustrated in Fig. 5. The clock set message (CSM) 500 includes a message type identification field 502 which distinguishes the clock set message CSM from other types of messages transmitted on control bus 214. In addition, the clock set

message (CSM) 500 includes a reference system frame number in field 506 (known as the reference system frame number field 504) and a reference master clock time in field 504 (known as the reference master clock time field 506). The reference master clock time field 506 specifies the reference master clock time in a format of hour, minute, and seconds (hh.mm.ss). If the control bus 214 employs addressing rather than dedicated connections between the master device board 200_M and the various slave boards 200_{S1} - 200_{Sn}, then an address field is also required in clock set message (CSM) 500. Other fields may also be included, e.g., parity or checksum fields, for example.

In a first mode of the invention, the clock set message (CSM) 500 directs the recipient slave processors 202_S to set their respective slave clocks 206_S to a specified real time (as specified in the reference master clock time field 506) upon the recipient processors detecting that their respective SFN counter 220 has reached a count equal to the value included in the reference system frame number field 504 (e.g., SFN=X in the illustrated example).

The first mode of the invention is illustrated in Fig. 4A, wherein at step 4A-1 master processor 202_M prepares and sends (via interface 212_M and over control bus 214) a clock set message (CSM) 500 having the format shown in Fig. 5. Step 4A-2 of Fig. 4A shows a slave processor 202_S receiving and processing the clock set message (CSM) 500, which involves, e.g., storing the values received in the reference system frame number field 504 and reference master clock time field 506. The SFN oscillator 210 continues to apply system frame signals (pulses) on SFN signal line 216, so that eventually (at step 4A-3) a pulse which would be counted as SFN =X is emitted. The slave processors 202_S monitor the counts of the system frame pulses maintained by their respective SFN counters 220. As indicated by step 4A-4, when the tally in a SFN counter 220 reaches the value included in the reference system frame number field 504 (e.g., SFN=X), the associated slave processor 202 resets its slave clock 206_S to the time specified in the clock set message (CSM) 500. Thus, when the counted number of system frame number signals as maintained by SFN counter 220 has a predetermined relationship with the value in reference system frame number field 504, the slave clock 206_S is reset to the hh.mm.ss value carried in the reference master clock time field 506. In other words, upon reaching the SFN=X as specified in the reference system frame

number field 504, the slave clock 206_S is reset to the actual time specified in the reference master clock time field 506 of the clock set message (CSM) 500.

In a second mode of the invention, the clock set message (CSM) 500 advises the recipient processors on the slave boards 200_{S1} - 200_{Sn} that an actual master clock time (as specified in reference master clock time field 506) occurred at the reference system frame number carried in the reference system frame number field 504. In this second mode, the recipient processor calculates an adjusted slave clock time at which its associated slave clock 206_S is to be reset.

The second mode of the invention is illustrated in Fig. 4B, wherein at step 4B-1 master processor 202_M prepares and sends (via interface 212_M and over control bus 214) a clock set message (CSM) 500 having the format shown in Fig. 5. Step 4B-2 of Fig. 4B shows a slave processor 202_S receiving and processing the clock set message (CSM) 500, which involves, e.g., storing the values received in the reference system frame number field 504 and reference master clock time field 506. Step 4B-3 shows the SFN oscillator 210 applying a system frame signal (pulse) on SFN signal line 216 which would be counted as SFN = Y. Then, knowing that the current system frame number SFN = Y, at step 4B-4, the slave processor 202_S calculates an adjusted slave clock time using the current system frame number SFN = Y, the value in reference system frame number field 504, and actual time value in the reference master clock time field 506. The adjusted slave clock time computed at step 4B-4 is thus not the actual time value in the reference master clock time field 506, but another value computed using the actual time value in the reference master clock time field 506. In other words, knowing that the actual time of master clock 206_M was the value stored in the reference master clock time field 506 at the particular system frame number stored in the reference system frame number field 504, the slave processor 202 can compute the master clock time at the current system frame number SFN =Y. The computation is simplified by the fact that the pulses of the system frame on line 216 occur at known intervals (e.g., every 10 milliseconds in the illustrated embodiment). With the adjusted slave clock time having been computed at step 4B-4, at step 4B-5 the slave processor 202 sets its associated slave clock 206_S to the adjusted slave clock time, thereby achieving synchronization.

While Fig. 4B happens to depict the transmission of the system frame signal amounting to SFN=Y (step 4B-3) subsequently to the sending of the clock set message

(CSM) 500 at step 4B-1, it should be understood that step 4B-3 may precede step 4B-1 in Fig. 4B. In other words, what is important in the second mode of the invention is that the slave processor 202 know the current system frame number at the time of making the computation of step 4B-4. Whether knowledge or updating of that current system frame number is acquired before or after receipt of clock set message (CSM) 500 is not material, as long as an accurate current system frame number is utilized.

Fig. 3 provides a second representative example embodiment for illustrating the real time clock synchronization of the present invention. In particular, Fig. 3 illustrates a scenario in which radio network controller (RNC) 24 maintains master clock 306_M which is used for synchronization of slave clocks 306_S situated at one or more base stations 22_1 - 22_q.

The master clock master clock 306_M is situated on a timing board 300_T of radio network controller (RNC) 24, and particularly is part of real time operating system (RTOS) 304_T of processor 302_T situated on timing board 300_T. In like manner as master board 200_M in Fig. 2, the timing board 300_T includes an interface 312_T through which processor 302_T communicates over control lines 314 with processors of the base stations 22. Also, timing board 300_T has a SFN oscillator 310 which outputs the system frame signals (pulses) in like manner as SFN oscillator 210 of Fig. 2.

Timing board 300_T is shown as having a port 313_T through which communications are established with the remainder of radio network controller (RNC) 24 via switch 315. Information of various types is transmitted between timing board 300_T and switch 315 through port 313_T, including the system frame signals and reset signals corresponding to those carried by lines 216 and 222 in Fig. 2. The switch 315 serves to connect differing units of radio network controller (RNC) 24, such units including (in addition to timing board 300_T) a diversity handover unit 340, a control node interface 342 (for interfacing, e.g., to MSC 26 or SGSN 25), and base station interfaces 344_1 - 344_q (which are connected, e.g., by landlines, to respective base stations 22_1 - 22_q).

Each base station 22 is connected via an extension board 350 to the radio network controller (RNC) 24. As explained previously, the extension board 350 is just one of several types of device boards which can be situated at a base station 22. The

extension board 350 receives the system frame signals from SFN oscillator 310_T and reset signals from processor 302_T of radio network controller (RNC) 24, and in one embodiment applies such signals via switch 352 to each of plural device boards 200 of base station 22. In Fig. 3, base station 22_1 is shown as having device boards $200_{1\text{-}S1}$ through $200_{1\text{-}Sn}$, base station 22_q is shown as having device boards $200_{q\text{-}S1}$ through $200_{q\text{-}Sk}$.

The device boards 200 of the base stations 22 of Fig. 3 are similar to those of Fig. 2, with the exception that each device board 200 has a port 354 as illustrated by port $354_{1\text{-}S1}$ of device board $200_{1\text{-}S1}$ and port $354_{q\text{-}S1}$ of device board $200_{q\text{-}S1}$. The ports 354 manage communications between switch 352 and constituent units of the device board 200, including SFN counter 220 and processor 202. In addition, for each device board 200 the processor 202 is connected via interface 212 to its respective control line 314. Control line 314 carries the clock set message (CSM) 500, which for the embodiment of Fig. 3 can have a same example format as shown in Fig. 5 and discussed above.

In the Fig. 3 embodiment, each of the device boards 200 at each base station 22 can have their slave clocks 206 synchronization directly in the manner depicted by device board $200_{1\text{-}S1}$ and above described with respect to either the mode of Fig. 4A or the mode of Fig. 4B. That is, each device board 200 can receive the system frame signals from the SFN oscillator 310_T of radio network controller (RNC) 24 and the clock set message (CSM) 500 from radio network controller (RNC) 24. In this case, the control line 314 is connected to each device board 200 in the base station which has a slave clock 106 requiring synchronization, and an address field is required in the clock set message (CSM) 500 for specifying the particular device board 200 at base station 22 to which the clock set message (CSM) 500 is applied.

Alternatively, the master clock 306_T of radio network controller (RNC) 24 can first be used to synchronize a predetermined slave clock 206 of one of the device boards 200 at each base station (e.g., device board $200_{1\text{-}S1}$ at base station 22_1), with the first-synchronized such slave clock 206 then serving as an assistant master clock for synchronizing the remaining slave clocks 206 on other device boards 200 of the same base station 22. After the initial synchronization, the assistant master clock is supervised and phase corrected by the radio network controller (RNC) 24. In this

alternate operation, each device board 200 of a base station 22 receives the system frame signals directly from the SFN oscillator 310_T, but the clock set message (CSM) 500 is relayed from the device board 200 having the first-synchronization slave clock to other boards at the base station 22 for the synchronization of the remaining slave clocks on the other device boards 200.

As mentioned above, the clock set message (CSM) 500 for the embodiment of Fig. 3 can operate in either the mode of Fig. 4A or the mode of Fig. 4B. Such modes are understood with reference to the preceding discussion of Fig. 2.

The embodiment of Fig. 3 has been illustrated with the nodes employing switches for routing information through the nodes. Examples of such switches can be ATM switches for routing ATM cells through nodes. It should be understood that other types of routing techniques may be utilized, as desired, or that (alternatively) the signals here pertinent can be directly or otherwise applied from radio network controller (RNC) 24 to an appropriate device board 200 in a base station 22. Furthermore, it should be understood that intra-node switches may also be used in the embodiment of Fig. 2, although not specifically illustrated herein.

From the foregoing it may also be understood how the master processor, and hence the master clock, can be located at a control node of the telecommunications network 18, such as mobile switching center 26. In such event, the master processor is employed to reset slave clocks at inferior nodes (e.g., radio network controller (RNC) 24 and/or the base stations 22).

Advantageously, the present invention facilitates accurate synchronization of real time clocks at a node, and even among plural nodes of telecommunications network 18 by capitalizing upon another feature (SFN) of the telecommunications network 18. Thus, the synchronization of the present invention allows real time operating systems (RTOS) to time stamp events occurring in telecommunications network 18 with precision. These events can be, for example, alarm reports sent to other nodes or log events recorded in a log file for use, e.g., when de-bugging the system.

While the invention has been described in connection with what is presently considered to be the most practical and preferred embodiment, it is to be understood that the invention is not to be limited to the disclosed embodiment, but on the contrary, is intended to cover various modifications and equivalent arrangements included within the spirit and scope of the appended claims.

WHAT IS CLAIMED IS:

1. A telecommunications network comprising:

a master processor having a master clock;

a recipient processor having a slave clock;

a source of system frame number signals which are applied to the recipient processor;

wherein the master processor sends a clock set message to a recipient processor, the clock set message including a reference master clock time and a reference system frame number; and

wherein the recipient processor resynchronizes the slave clock using the reference master clock time and the reference system frame number.

2. The apparatus of claim 1, wherein the clock set message directs the recipient processor to set the slave clock to a specified real time upon the recipient processor obtaining the reference system frame number.

3. The apparatus of claim 2, further comprising a counter which counts the system frame number signals at the recipient processor; and wherein the recipient processor, when a counted number of system frame number signals has a predetermined relationship with the reference system frame number, sets the slave clock to the reference master clock time.

4. The apparatus of claim 1, wherein the clock set message advises the recipient processor of an actual master clock time at the reference system frame number, thereby enabling the recipient processor to calculate an adjusted slave clock time.

5. The apparatus of claim 1, wherein the master processor and the recipient processor are located at a same node of the telecommunications network.

6. The apparatus of claim 5, wherein same node of the telecommunications network is a base station node.

7. The apparatus of claim 5, wherein the master processor and the recipient processor are located on differing device boards at a same node of the telecommunications network.

8. The apparatus of claim 1, wherein the master processor and the recipient processor are located at differing nodes of the telecommunications network.

9. The apparatus of claim 8, wherein the master processor is located at a radio network controller node and the recipient processor is located at a base station node of the telecommunications network.

10. The apparatus of claim 8, wherein the master processor is located at a radio network controller node; wherein a first recipient processor is located at a first base station node; and wherein a second recipient processor is located at a second base station node.

11. The apparatus of claim 1, wherein the source of system frame number signals is an oscillator.

12. A method of operating a cellular telecommunications system of the type wherein a master processor maintains a master clock and wherein system frame numbers are utilized, the method comprising:

the master processor sending a clock set message to a recipient processor, the clock set message including a reference master clock time and a reference system frame number;

the recipient processor resynchronizing the slave clock using the reference master clock time and the reference system frame number.

13. The method of claim 12, wherein the clock set message directs the recipient processor to set the slave clock to a specified real time upon the recipient processor obtaining the reference system frame number.

14. The method of claim 13, further comprising:

periodically sending system frame number signals to the recipient processor;

counting the system frame number signals at the recipient processor; and, when a counted number of system frame number signals has a predetermined relationship with the reference system frame number,

setting the slave clock to the reference master clock time.

15. The method of claim 12, wherein the clock set message advises the recipient processor of an actual master clock time at the reference system frame number, thereby enabling the recipient processor to calculate an adjusted slave clock time.

16. The method of claim 15, further comprising:

preparing the clock set message whereby the reference master clock time in the clock set message refers to the actual master clock time at a time when the system frame number was the reference system frame number;

periodically sending system frame number signals to the recipient processor;

maintaining a current count of the system frame number signals at the recipient processor; and,

calculating the adjusted slave clock time using the current count of the system frame number signals, the reference system frame number, and the reference master clock time.

17. The method of claim 12, further comprising locating the master processor and the recipient processor at a same node of the telecommunications network.

18. The method of claim 17, wherein same node of the telecommunications network is a base station node.

19. The method of claim 12, further comprising locating the master processor and the recipient processor on differing device boards at a same node of the telecommunications network.

20. The method of claim 12, further comprising locating the master processor and the recipient processor at differing nodes of the telecommunications network.

21. The method of claim 20, further comprising locating the master processor at a radio network controller node and locating the recipient processor at a base station node of the telecommunications network.

22. The method of claim 20, further comprising:

locating the master processor is located at a radio network controller node;

locating a first recipient processor at a first base station node; and

locating a second recipient processor at a second base station node.

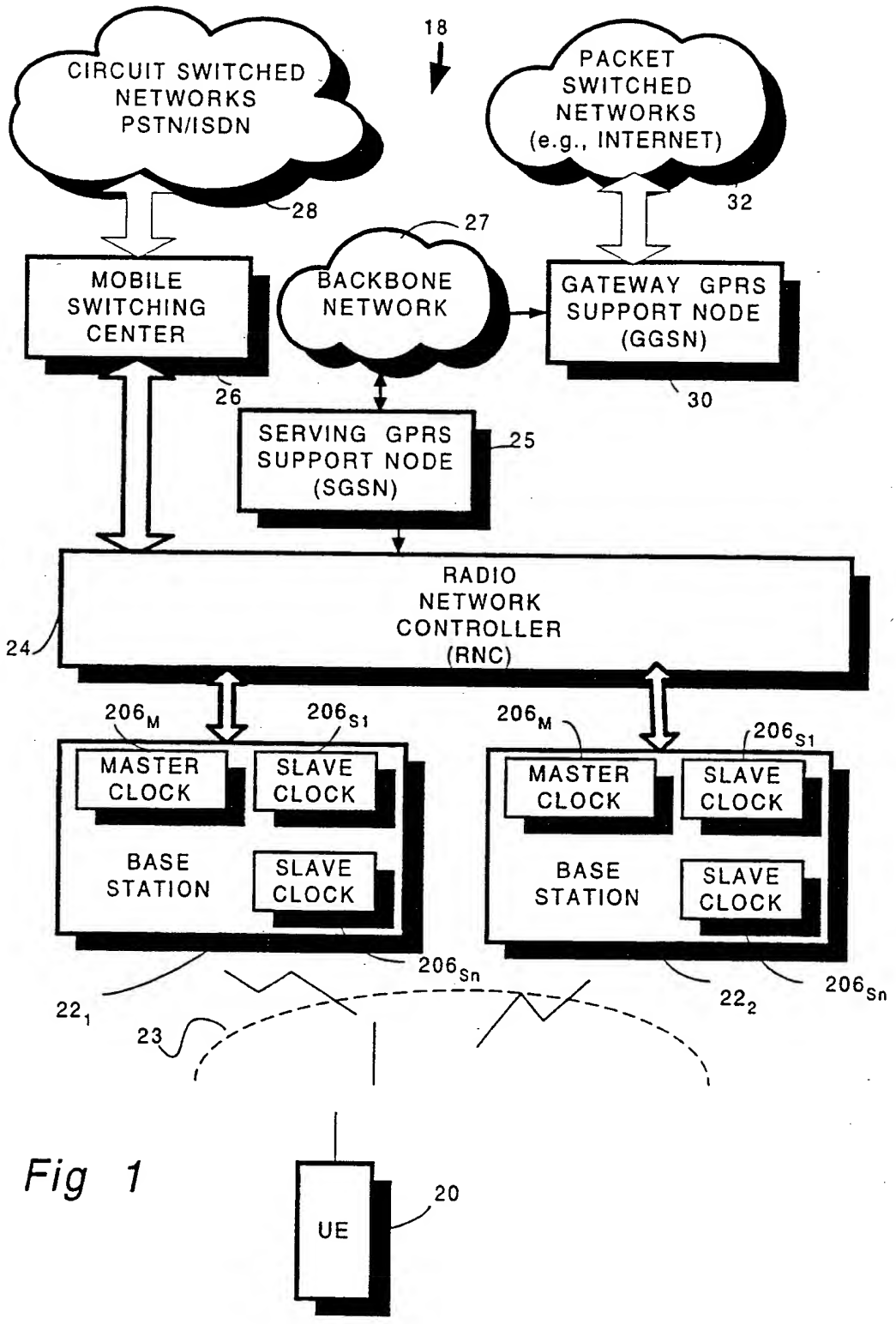

Fig 1

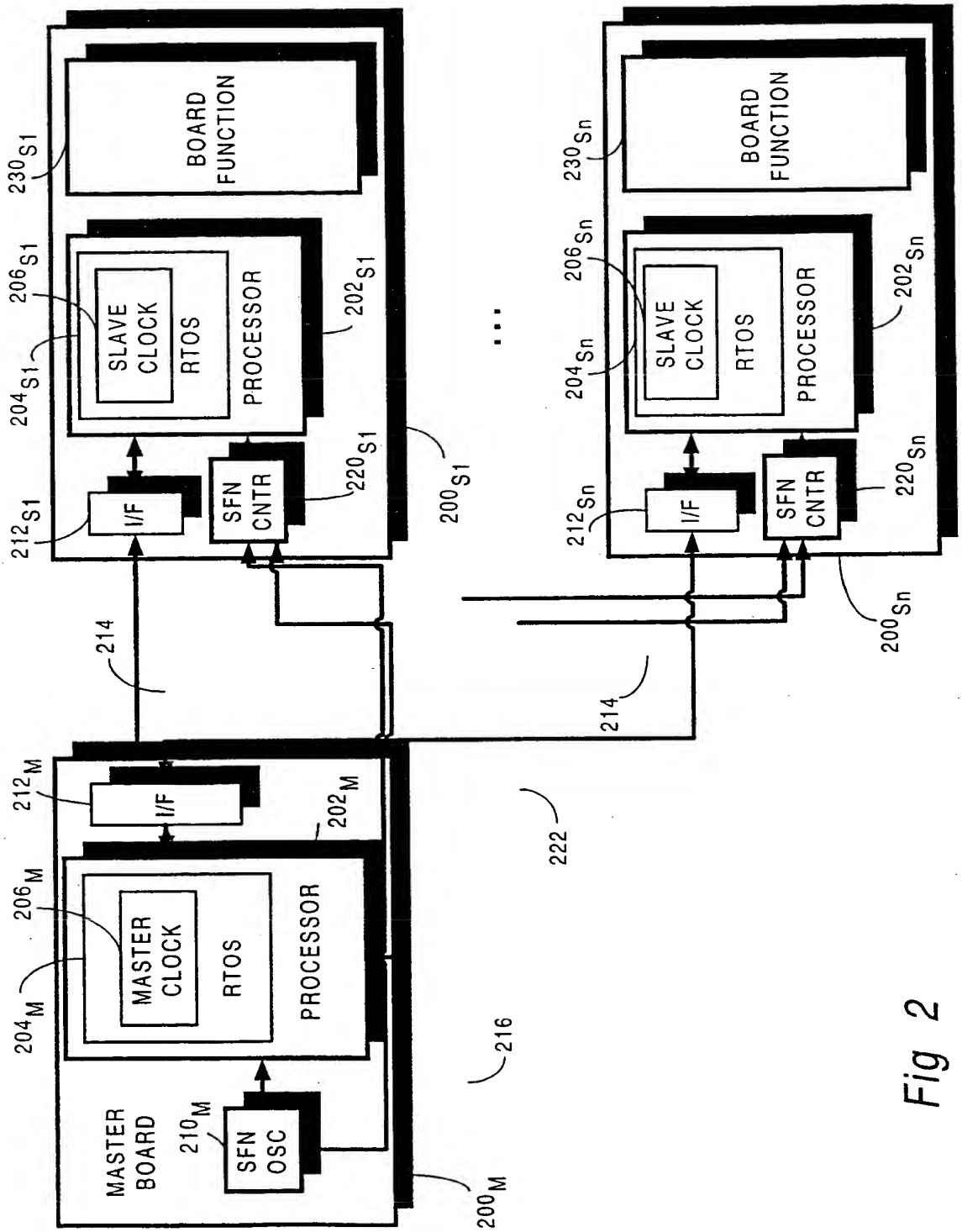

Fig 2

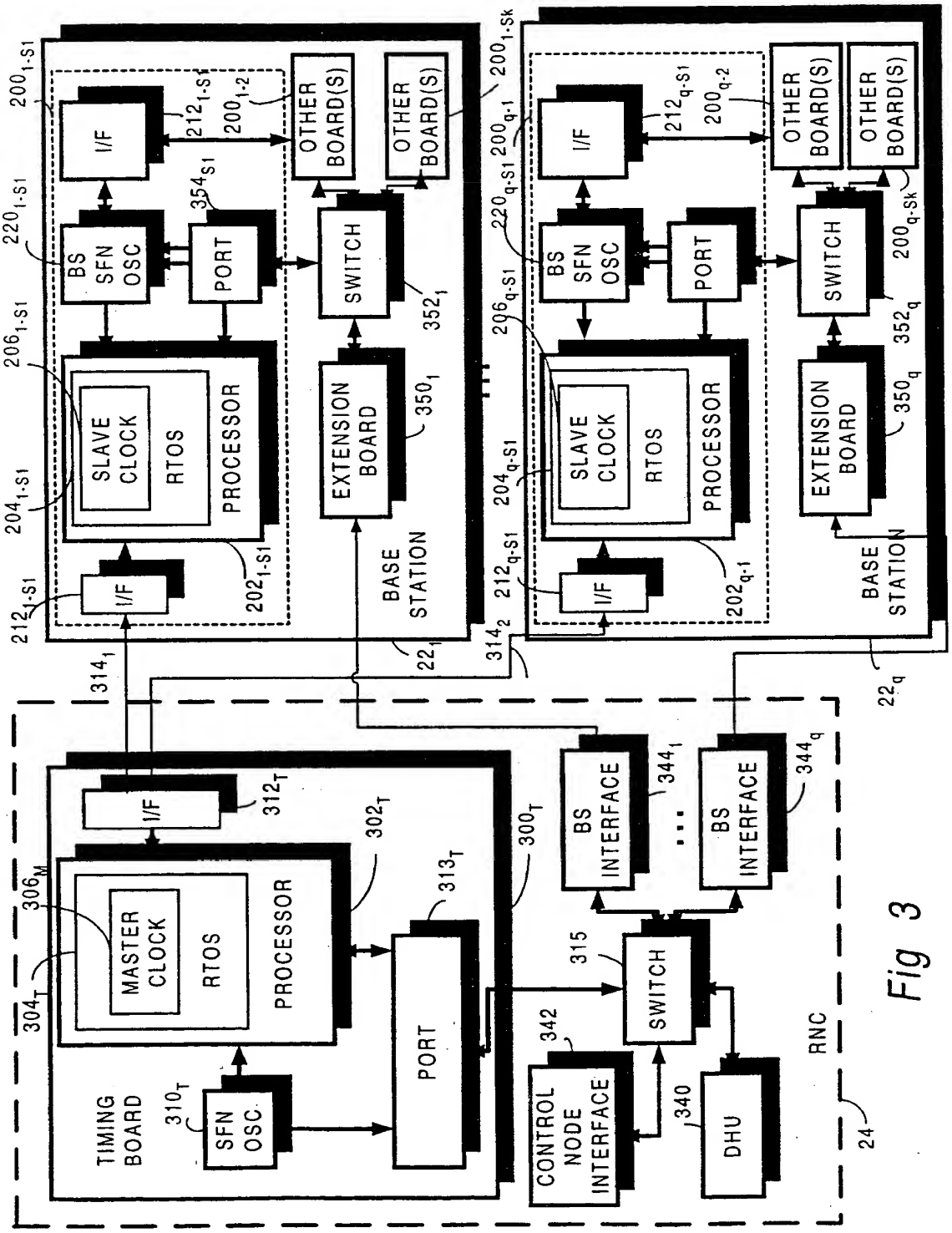

Fig 3

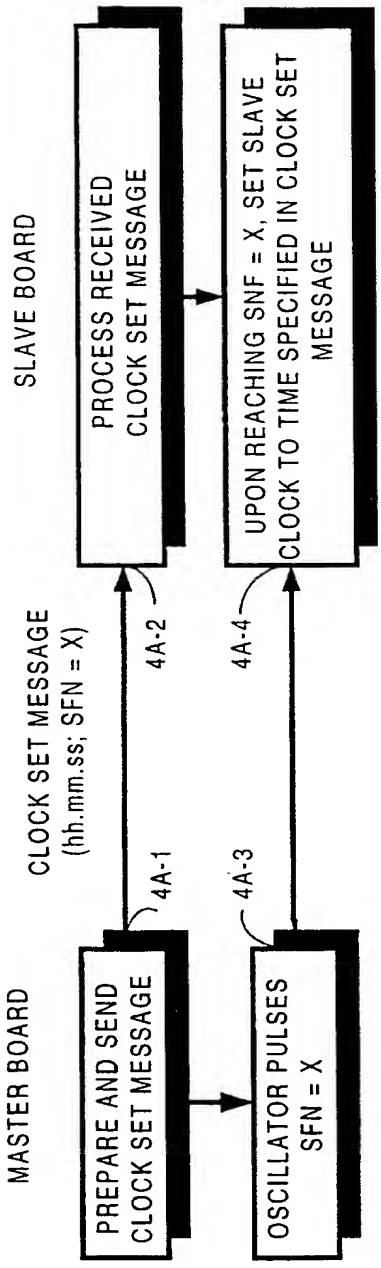

Fig 4A

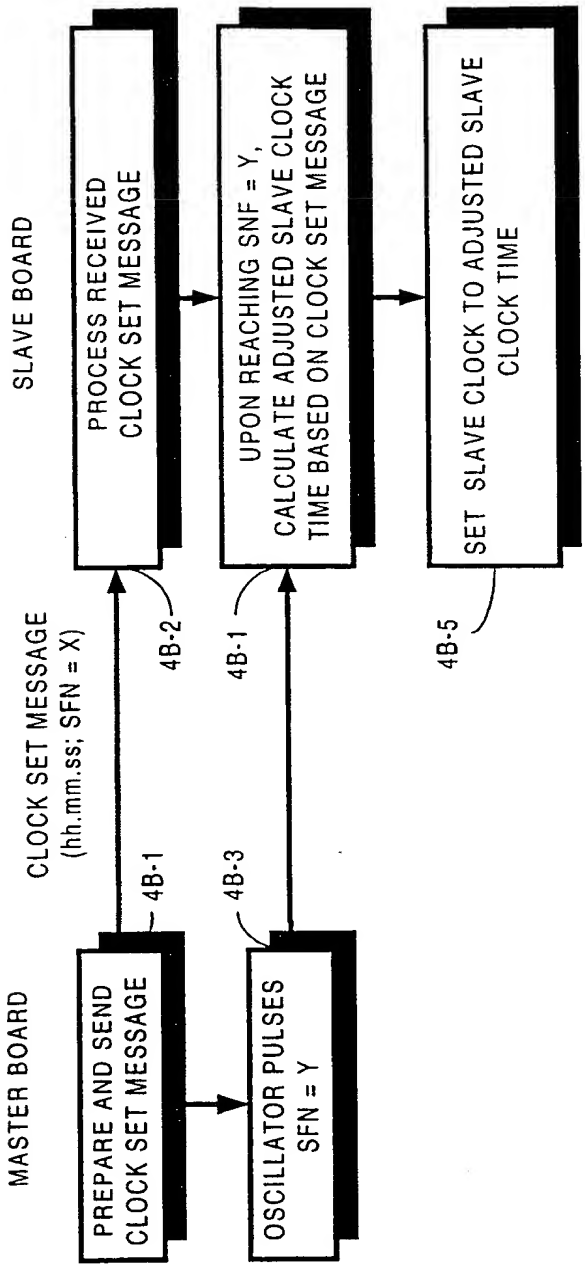

Fig 4B

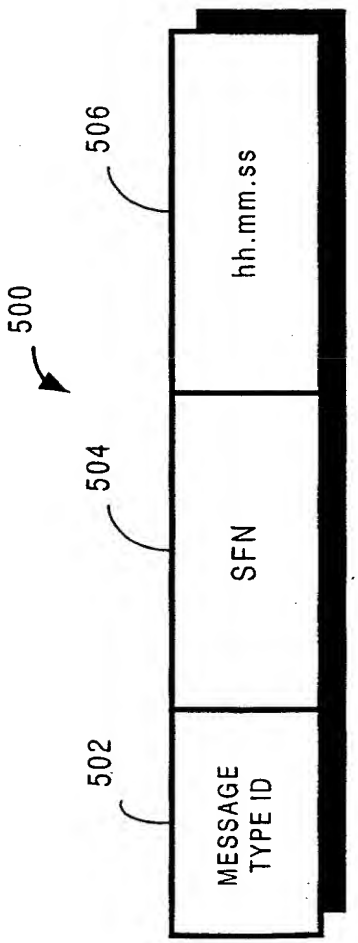

Fig 5

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SE 99/02416

A. CLASSIFICATION OF SUBJECT MATTER

IPC7: H04J 3/06, H04Q 9/00
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC7: H04Q, H04J, H04L

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C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 4337463 A (R.F. VANGEN), 29 June 1982 (29.06.82), see abstract and claims	1-22
A	US 4530091 A (G.B. CROCKETT), 16 July 1985 (16.07.85), see abstract and claims	1-22
A	US 3798650 A (A.D. MCCOMAS ET AL.), 19 March 1974 (19.03.74), see abstract and claims	1-22
A	US 6009530 A (B.J. GOATLY), 28 December 1999 (28.12.99), see abstract and claims	1-22

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

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Information on patent family members

International application No.
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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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		GB 1410396 A	15/10/75
US 6009530 A	28/12/99	NONE	

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(74) Agent: NORIN, Klas; Ericsson Radio Systems AB, Common Patent Department, S-164 80 Stockholm (SE).

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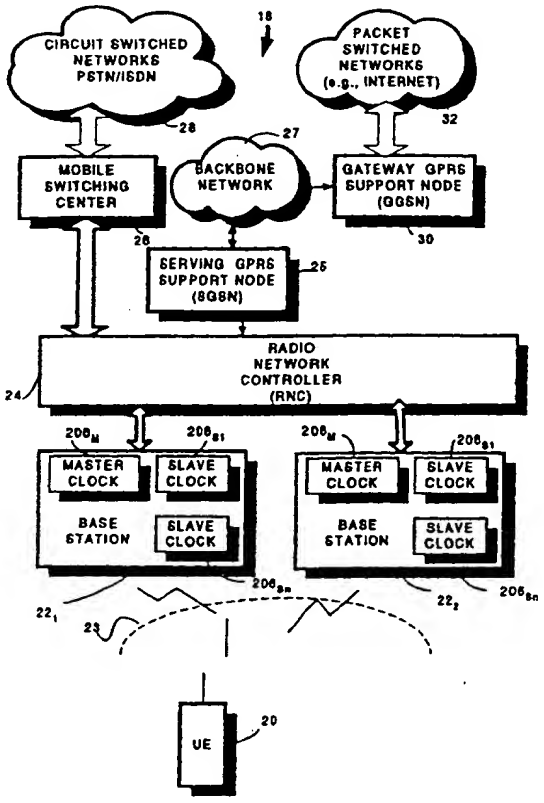
(54) Title: CLOCK SYNCHRONIZATION IN TELECOMMUNICATIONS NETWORK USING SYSTEM FRAME NUMBER

(57) Abstract

A telecommunications system (18) capitalizes employment of a system frame number (SFN) for synchronizing plural real time clocks (206) provided at one or more nodes of the network. System frame signals (e.g., pulses) are distributed from a source (210, 310) to processors (202) having slave clocks (206_S) that need to be synchronized with a master clock. A master processor (202_M, 302_T) sends a clock set message (500) to the processors, the clock set message including a reference master clock time (506) and a reference system frame number (504). The recipient processors which receive the clock set message resynchronize their respective slave clocks using the reference master clock time and the reference system frame number. In one mode, the clock set message directs the recipient processors to set their respective slave clocks to the reference master clock time upon the recipient processors obtaining the reference system frame number. In another mode, the clock set message advises the recipient processors of an actual master clock time at the reference system frame number, thereby enabling the recipient processor to calculate an adjusted slave clock time.



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